# □ MN101C74D , MN101C74F, MN101C74G

Туре	MN101C74D(underdevelopment)	MN101C74F (under planning)	MN101C74G (under development)			
ROM (×8-bit)	64 K	96 K	128 K			
RAM (×8-bit)	2 K	6 K	6 K			
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free (under planning), MLGA100-L-1010 *Lead-free (under planning)					
Minimum Instruction Execution Time	0.1 µs (at 3.0 V to 3.6 V, 10 MHz) 0.235 µs (at 1.8 V to 3.6 V, 4.25 MHz) 62.5 µs (at 1.8 V to 3.6 V, 32 kHz) * The lower limit for operation guarantee for flash memory built-in type is 2.2 V.					
Interrupts		• External 1 • External 2 • External 3				
	• External 6 (key interrupt dedicated) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Time base • Timer 7 (2 systems) • Timer 8 (2 systems) • Serial 0 (2 systems) • Serial 1 (2 systems) • Serial 3 • A/D conversion finish • Automatic transfer finish					
Timer Counter	measurement, added pluse (2-bit) s possible) Clock source 1/ cl	vent count, generation of remote contro system PWM output) (square-wave/PW /2, 1/4 of system clock frequency; 1/1, ock frequency; 1/1 of XI oscillation clo pincidence with compare register 0	M output to large current terminal PC3 1/4, 1/16, 1/32, 1/64 of OSC oscillation			
	Timer counter 1 : 8-bit × 1 (square-wave output, event count, synchronous output event) Clock source					
	Interrupt source coincidence with compare register 1					
	Timer counter 0, 1 can be cascade-connected.					
	count, synchronous output event, s terminal PC5 possible) Clock source 1/ cl	2-bit) system PWM output, PWM outp imple pulse width measurement) (squar 2, 1/4 of system clock frequency; 1/1, ock frequency; 1/1 of XI oscillation clo pincidence with compare register 2	re-wave/PWM output to large current 1/4, 1/16, 1/32, 1/64 of OSC oscillation			
	Clock source ······ 1/ cl	generation of remote control carrier, ser /2, 1/8 of system clock frequency; 1/1, ock frequency; 1/1 of XI oscillation clo pincidence with compare register 3	1/4, 1/16, 1/64, 1/128 of OSC oscillation			
	Timer counter 2, 3 can be cascade-co	onnected.				
	fr	/1 of system clock frequency; 1/1, 1/128 equency; 1/1, 1/128, 1/8192 of XI oscil pincidence with compare register 6				
	Timer counter 7 : 16-bit × 1 (square-wave output, 16-bit PWM o pulse width measurement, input ca be changed constantly)) (square-w Clock source	output (cycle / duty continuous variable pture, real time output control, high pe ave/PWM output to large current termin '1, 1/2, 1/4, 1/16 of system clock freque scillation clock frequency; 1/1, 1/2, 1/4 pincidence with compare register 7 (2 li	rformance IGBT output (Cycle/Duty ca nal PC4 possible) ency; 1/1, 1/2, 1/4, 1/16 of OSC , 1/16 of external clock input frequency			

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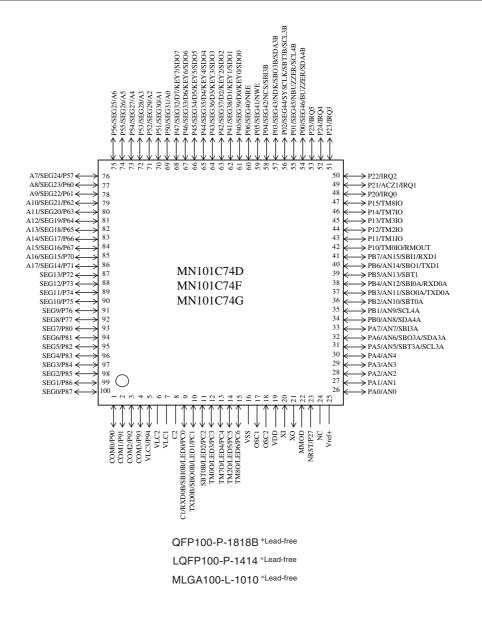
Timer Coun	ter (Continue)	Timer counter 8: 16 bit × 1 (square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture) (square-wave/PWM output to large current terminal PC6 possible) Clock source					
		Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM is possible as a 32-bit timer.) Time base timer (one-minute count setting) Clock source					
		Watchdog timer Interrupt source					
DMA Contro (Automatic I	ller Data Transfer)	Max. Transfer cycles255Starting factorexternal request, various types of interrupt, softwareTransfer mode1-byte transfer, word transfer, burst transfer					
Serial Interface		Serial 0 : synchronous type/UART (full-duplex) × 1 Clock source					
		Serial 3 : synchronous type/single-master I <sup>2</sup> C × 1 Clock source					
		Serial 4 : I <sup>2</sup> C slave × 1 Applicable for I <sup>2</sup> C high-speed transfer mode, 7-bit/10-bit address setting, general call					
I/O Pins	I/O	87 • Common use • Specified pull-up resistor available • Input/output selectable (bit unit)					
A/D Inputs		$10$ -bit $\times$ 16-ch. (with S/H)					
LCD		47 segments × 4 commons (static, 1/2, 1/3, or 1/4 duty) LCD power supply separated from VDD (usable if VDD ≤ VLCD ≤ 3.6 V) LCD power step-up circuit contained (3/2, 2 and 3 times) LCD power shunt resistance contained LCD reference voltage is contained.					
Special Port	S	Buzzer output, remote control carrier signal output, high-current drive port					
<b>ROM Correction</b> Correcting address designation: up to 7 addresses possible		Correcting address designation: up to 7 addresses possible					

#### Electrical Characteristics

#### Supply current

Parameter	Symbol	Condition	Limit			Unit
raiaiilelei		Condition		typ	max	Unit
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		1	1.8	mA
	IDD2	fx = 32 kHz, VDD = 3 V		4	15	μA
Cumply aureant at HALT	IDD3	fx = 32 kHz, VDD = 3 V, Ta = 25°C		2	5	μA
Supply current at HALT	IDD4	$fx = 32 \text{ kHz}, \text{VDD} = 3 \text{ V}, \text{ Ta} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$			10	μA
Supply automated STOD	IDD5	$VDD = 3 V, Ta = 25^{\circ}C$			2	μA
Supply current at STOP	IDD6	$VDD = 3 V, Ta = -40^{\circ}C to +85^{\circ}C$			8	μA

#### Pin Assignment



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## **Support Tool**

PX-ICE101C / D + PX-PRB101C74-QFP100-P-1818B-M (under development) PX-ICE101C / D + PX-PRB101C74-LQFP100-P-1414-M (under planning)	
Туре	MN101CF74G (under development)
ROM (× 8-bit)	128 K
RAM (× 8-bit)	6 K
Minimum instruction execution time	0.1 µs (at 3.0 V to 3.6 V, 10 MHz)
	$0.235\ \mu s$ (at 2.2 V to 3.6 V, 4.25 MHz)
	62.5 µs (at 2.2 V to 3.6 V, 32 kHz)
Package	QFP100-P-1818B *Lead-free, LQFP100-P-1414 *Lead-free (under planning)
	MLGA100-L-1010 *Lead-free (under planning)
	PX-ICE101C / D + PX-PRB101C74-L Type ROM (× 8-bit) RAM (× 8-bit) Minimum instruction execution time

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